REMARKS

I. FORMAL MATTERS

Applicant notes with appreciation the Examiner's indication that claims 1-4 are allowed.

Applicant notes with appreciation the Examiner's acknowledgement of the claim to foreign priority under 35 U.S.C. § 119(a)-(d) or (f) and indication that the certified copies of the priority documents have been received.

Applicant notes with appreciation the Examiner's indication that the formal drawings filed on July 24, 2001 are acceptable.

Applicant notes with appreciation the Examiner's inclusion of a copy of the PTO Form 1449 that was submitted with the Information Disclosure Statement filed on July 23, 2004. The reference listed therein is initialed by the Examiner, thereby indicating that this reference was considered by the Examiner and should be listed on any patent that issues from the present application.

II. PRIOR ART REJECTION

Claims 5-8 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Motegi (U.S. Patent No. 6,025,822). The Examiner's rationale is substantially similar to the rejection presented in the previous Office Action dated June15, 2004 with respect to claims 5-8. This rejection is traversed.

Claim 5

In response to Applicant's argument that the column drivers 21 of Motegi are not connected in series, the Examiner asserts that the column drivers 21 are connected in series with each other. Applicant respectfully submits that the Examiner is not correct. Specifically, Fig. 7 of Motegi clearly shows the column drivers 21 and row drivers 22 connected in parallel.

In fact, Figure 7 of Motegi corresponds to Figure 5 of the present specification, which illustrates a conventional liquid crystal display device. Both Figure 7 of Motegi and Figure 5 of the present invention show column drivers and row drivers that are connected in parallel. Therefore, Motegi merely shows the conventional art. The Examiner has continued to assert that Figure 7 of Motegi shows column drivers connected in series. However, this is not correct. Applicant has prepared the attached drawing to clearly illustrate the differences between parallel and serial connection. As shown in the attached drawing labeled "PARALLEL CONNECTION,"

which illustrates Figure 7 of Motegi and Figure 5 of the present application, the input signals clearly are applied in parallel to the column and row drivers. In contrast, in the attached drawing labeled "SERIAL CONNECTION," which illustrates the present invention, the input signal clearly is applied in series to the column and row drivers.

Therefore, Motegi fails to teach or suggest a plurality of column electrode driving circuits connected in series and a plurality of row electrode driving circuits connected in series.

Figure 7 of Motegi shows that the controller 23 supplies signals 26 to the column drivers, and signal 25 to the row drivers. The signals sent from the controller 23 to the column drivers are described as display data, clocks for taking the display data, enable signals for activating column drivers, latch pulses for outputting data to the liquid crystal panel, voltages for liquid display to be applied to the liquid crystal panel by means of the column drivers and signals for transforming liquid crystal driving outputs into an alternating current form (see column 1, lines 60-67). The control signals from controller 23 to the row drivers are described as selection data, shift clocks for shifting the selection data, voltages for liquid crystal display to be applied to the liquid crystal display panel by means of the row drivers and signals for transforming liquid crystal display outputs into an alternating current form (see column 2, lines 1-6).

Also, Motegi fails to teach or suggest a timing signal for controlling an operation timing of the plurality of column electrode driving circuits and the plurality of row electrode circuits that is generated in the first column electrode driving circuit. The Examiner asserts that it would have been obvious to one skilled in the art at the time of invention to utilize the timing signal which is inherently included in the controller 23 of figure 7 in the column driver 21 closest to the row driver 23 in order to save space. The Examiner has failed to show any disclosure in any reference of why this would have been obvious to one skilled in the art at the time of the invention. It appears that the Examiner is using impermissible hindsight reasoning in coming to this conclusion. Additionally, under *In re Zurko*, the Examiner is required to provide evidence to support his arguments.

Further, Motegi fails to teach or suggest that the generated timing signal and a data signal are output to a second column electrode driving circuit . . . which is directly connected to the first column electrode driving circuit. There is no disclosure or suggestion anywhere in Motegi that a generated timing signal and a data signal is output to a second column driver from the first driver. In Figure 7 of Motegi, the column drivers are connected in parallel (as in the conventional art shown in Figure 5 of the present application). Therefore, it is impossible for the first column driver to send a data signal to the second column driver.

Still further, Motegi fails to teach or suggest that the generated timing signal is transferred in a cascading manner to the plurality of row electrode driving circuits as a

scanning signal. In Figure 7 of Motegi, the row drivers are connected in parallel and each receives signals from the controller 23. There is no disclosure or suggestion that a generated timing signal that has been generated in the first column driver is transferred in a cascading manner to the plurality of row drivers as a scanning signal.

It is also noted that in the Office Action dated June 15, 2004, the Examiner asserts that the controller 2 and level shifter circuit 14b of Figure 1 of Motegi are used to input to the first column electrode driver. However, as stated above, in the Examiner's response to amendment, the Examiner asserts that the timing signal is supplied from the controller 23 of Figure 7. First, Applicant submits that the Examiner's reasoning is unclear. Specifically, it is unclear if the Examiner means the controller 2 of Figure 1 or the controller 23 of Figure 7. Second, if the Examiner is relying on Figure 1 of Motegi, then as Figure 1 represents the invention of Motegi and Figure 7 represents prior art, the Examiner has not provided evidence of why the prior art would be combined with the invention of Motegi. Accordingly, the Examiner has failed to form a prima facie case of obviousness.

Thus Motegi fails to teach or suggest claim 5, and the Examiner has failed to show adequate support for his assertions of obviousness and thus fails to provide a prima facie case of obviousness. Therefore, claim 5 is distinguished over Motegi and the present rejections should be withdrawn.

Claim 6

In addition to claim 5, claim 6 recites the features "a timing signal which is output from the first column electrode driving circuit is supplied to the first row electrode driving circuit sequentially through a first line portion provided on the tape carrier package mounting the first column electrode driving circuit, a second line portion provided on the printed circuit board, a third line provided on the tags carrier package mounting the first column electrode driving circuit, and a fourth line portion provided on the display panel."

Motegi fails to teach or suggest the above features. The Examiner asserts that the above feature is taught in Figure 6 of Motegi. However, Figure 6 of Motegi does not show anything of the kind. Thus, the Examiner has failed to show teachings of claim 6 and thus the present rejection should be withdrawn.

Again the Examiner is combining the invention of Motegi (Figure 1) with the prior art of Motegi (Figure 7) without giving any indication of motivation for combining these.

Further, claim 6 would not have been obvious over Motegi for the reasons presented above with respect to claim 5.

Claim 7

Claim 7 recites "a plurality of column electrode driving circuits connected in series . . . a plurality of row electrode driving circuits connected in series ... wherein a timing signal for controlling the plurality of row electrode driving circuits is supplied to one of the plurality of row electrode driving circuits sequentially through a second line portion provided on the printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel."

Motegi fails to teach or suggest a timing signal for controlling the plurality of row electrode driving circuits that is supplied to one of the plurality of row electrode driving circuits sequentially through a second line portion provided on the printed circuit board, a third line portion provided on one of the plurality of column electrode driving circuits, and a fourth line portion provided on the display panel. The Examiner fails to point out where this feature is disclosed in Motegi.

Also, as presented above with respect to claims 5 and 6, Figure 7 of Motegi shows that both the column drivers 21 and the row drivers 22 are connected in parallel, not in series, as in the present invention.

Therefore, because Motegi fails to teach or suggest all of the feature of claim 7, the rejection of claim 7 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

Claim 8

Claim 8 recites "a signal circuit is provided to use for signals being different from a timing signal which is output from the first column electrode driving circuit . . . the timing signal which is output from the first column electrode driving circuit is supplied to the first row electrode driving circuit sequentially though the circuit board as not to be cross with the signal circuit."

In addition to the arguments presented above with respect to claim 5, Motegi also fails to teach or suggest the above features of claim 8. Specifically, Motegi does not disclose a signal circuit to use for signals being different from a timing signal which is output from the first column electrode driving circuit.

Therefore, because Motegi fails to teach or suggest all of the feature of claim 8, the rejection of claim 8 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

If the Examiner believes that any of the outstanding issues could be resolved by a telephone interview, the Examiner is kindly invited to call the undersigned at the listed telephone number.

Applicant believes that no additional fees are due for the subject application. However, if for any reason a fee is required, a fee paid is inadequate or credit is owed

for any excess fee paid, you are hereby authorized and requested to charge Deposit Account No. **04-1105**.

Respectfully submitted,

Date: March 28, 2005
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